9   a global video bus which routes the video data between said processing

10   module and said at least one video processing module; and

11   a global control bus which provides said control data to/from said

12   processing module from/to said at least one video processing module, said global

13   control bus being separate from said [video data on said] global video bus.

1   2.   (Amended)   The system of claim 1, wherein said video data is

2   coupled with associated video timing signals [information] synchronized to a system

3   clock signal, and each video processing module comprises a crosspoint switch

4   which routes said video data and its associated video timing signals [information]

5   to/from respective ones of the parallel pipelined video hardware components, said

6   timing [data] signals indicating when the video data represents active video

7   information [compensating for pipeline delay in said video processing module].

1   3.   (Amended)   The system of claim 2, wherein each video processing

2   module further comprises a crosspoint switch state machine which monitors

3   transfers of video data over each data path of said crosspoint switch and facilitates

4   [selection of idle data] allocating paths for [each transfer of data from one]

5   transferring the video data among the parallel pipelined video hardware [component

6   to another] components.

1   4.   (Amended)   The system of claim 2, wherein at least one video

2   processing module comprises a configurable arithmetic logic unit (CALU)

3   responsive to said video data and its associated video timing [information] signals

4   so as to automatically compensate for differences in input video timing between

5   respective images and to provide dual image pointwise video processing operations

6   and image accumulations.

1   5.   (Amended)   The system of claim 2, wherein at least one video

2   processing module comprises at least one pyramid filtering processor which

3   generates [pyramid] spatially filtered representations of the video data at

4   respectively different resolutions so as to facilitate real-time processing of said

5   video data [for said particular image processing tasks of said video processing

6   system].

1   6.   (Amended)   The system of claim 2, wherein <u>the modular video</u>

2   <u>processing system includes a plurality of video processing modules and each video</u>

3   <u>processing module comprises a connection</u> for at least one daughterboard [which

4   performs a video processing function on said video data which is unique to

5   particular image processing tasks of said video processing system] <u>the connection</u>

6   <u>including means for routing at least a portion of the control data between the</u>

7   <u>processing module and the daughterboard and for coupling the daughterboard to the</u>

8   <s>crosspoint switch.</s>

1   7.   (Amended)   The system of claim 6, [wherein said at least one]

2   <u>further including a</u> daughterboard [comprises] <u>comprising</u> a display processor card

3   <u>coupled to the daughterboard connection of one of the plurality of video processing</u>

4   <u>modules, the display processor card</u> including video input [and output] ports

5   connected to said crosspoint switch and an encoder which converts video data

6   received at [an] <u>at least one of the</u> input [port] <u>ports</u> into a video signal of a

7   predetermined format for display.

1   8.   (Amended)   The system of claim 6, [wherein said at least one]

2   <u>further including a</u> daughterboard [comprises] <u>comprising</u> a digitizer card <u>coupled</u>

3   <u>to the daughterboard connection of one of the plurality of video processing</u>

4   <u>modules, the digitizer card</u> including video [input and] output ports connected to

5   said crosspoint switch and a decoder which decodes and digitizes video data

6   received at [an] <u>at least one</u> input port into a video signal of a predetermined format

7   [for further processing so as to provide an input and output interface for digital

8   video] <u>and provides the digitized video data to at least one of the output ports</u>.

1   9.   (Amended)   The system of claim 6, [wherein said at least one]

2   <u>further including a</u> daughterboard [comprises] <u>comprising</u> a correlator card <u>coupled</u>

3   <u>to the daughterboard connection of one of the plurality of video processing</u>

4   modules, the correlator card including a plurality of video input and output ports

5   connected to said crosspoint switch and a plurality of video processing channels,

6   each channel comprising a configurable arithmetic logic unit, a pyramid filtering

7   processor, and a look up table [which correlate respective images in each video

8   processing channel in a predetermined manner].

              19   *17*

1   10.   (Amended) The system of claim 6, [wherein said at least one]

2   further including a daughterboard [comprises] comprising a warper card coupled to

3   the daughterboard connection of one of the plurality of video processing modules,

4   the warper card including video input and output ports connected to said crosspoint

5   switch, [and an address generator and] a pair of memory banks, an address

6   generator, for controlling memory read operations and memory write operations in

7   the memory banks, and a bilinear interpolator [for parametric transformation of

8   video data received at an input port].

            20   *19*

1   11.   (Amended) The system of claim [6] 10, wherein said [at least one

2   daughterboard comprises a warper card including a plurality of video input and

3   output ports connected to said crosspoint switch, a pair of memory banks, and a

4   plurality of] address generator and said bilinear interpolator are implemented as at

5   least one field programmable gate array [arrays programmed so as to provide

6   parametric transformation of video data received at said input ports].

1   12.   (Amended) The system of claim 1, wherein said processing

2   module comprises at least two microprocessors each of which has an associated

3   random access memory which is not shared with any other microprocessor, [and]

4   said processing module further comprising a shared memory which is accessible by

5   each microprocessor of said processor module through an arbitrated control bus

6   which arbitrates requests for access to said shared memory from each

7   microprocessor.

1   13.   (Amended) The system of claim 12, wherein said processing

2   module includes means for using the control data to program the at least one video

3   processing module to perform at least one of the different video processing
4   operations on the video data and means for providing a [provides at least one]
5   synchronous start signal to begin the at least one video processing operation [for
6   each different video processing operation of each video processing module].

1   _14._   *5* *3* (Amended)   The system of claim *12*, wherein said processing
2   module further comprises a communications [devices] interface for communicating
3   with external devices, said communications [devices] interface being [accessed by
4   each of said microprocessors via] coupled to said arbitrated control bus for access
5   by each of said at least two microprocessors.

1   *6* _15._   *3* (Amended)   The system of claim *12*, wherein said random access
2   memory associated with each microprocessor is connected to said global video bus
3   [and stores] to store video data for transmission to, and [stores] video data received
4   from [said at least one video processing module over] said global video bus.

1   *7* _16._   *3* (Amended)   The system of claim *12*, wherein said processor
2   module further comprises a semaphore register [available to each microprocessor
3   via] coupled to said arbitrated control bus, said semaphore register storing
4   semaphores so as to facilitate coordination of [and mutual exclusion of] mutually
5   exclusive operations by said at least two microprocessors.

1   17.   (Amended)   The system of claim 1, further comprising a hardware
2   control library loaded on a general purpose microprocessor of said processing
3   module, said hardware control library comprising a set of functions for
4   programming the parallel pipelined video hardware of said at least one video
5   processing module to perform [predetermined] respective ones of said different
6   video processing operations concurrently.

1   *9* _18._   *8* (Amended)   The system of claim *17*, wherein said processing
2   module comprises at least two general purpose microprocessors and said hardware
3   control library further comprises a set of functions for coordinating concurrent

4 multitask processing operations of said at least two general purpose

5 microprocessors.

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1   19.   (Amended)   The system of claim 17, wherein said control data

2 comprises [video device information] <u>respective control signals</u> for each hardware

3 component of said video processing system, wherein said functions of said

4 hardware control library manipulate said [video device information] <u>control signals</u>

5 to program said hardware components for each of said different video processing

6 operations.

1   20.   (Amended)   A method of creating a modular video processing

2 system, comprising the steps of:

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3   <u>providing video data via a global video bus;</u>

4   <u>providing a global control bus;</u>

5   connecting [to a global control bus] a processing module containing at least

6 one general purpose microprocessor <u>to said global video bus and said global control</u>

7 <u>bus</u> [which controls] <u>said microprocessor controlling</u> hardware and software

8 [operation] <u>operations</u> of said video processing system using control data <u>and</u>

9 <u>processing said video data;</u>

10   connecting to said global control bus <u>and said global video bus to</u> at least

11 one video processing module which contains parallel pipelined video hardware

12 [which is programmable by] <u>that is responsive to</u> said control data to provide

13 different video processing operations on [an input stream of] <u>the</u> video data;

14   <u>wherein</u> said processing module [detecting] <u>detects</u> the presence of each

15 video processing module connected to said global control bus; and [said processing

16 module passing] <u>passes</u> said control data to each detected video processing module

17 over said global control bus to program said parallel pipelined video hardware to

18 perform [a video processing function which is unique to particular processing tasks

19 of said video processing system] <u>at least one of said video processing operations.</u>

1   21.   (Amended) The method of claim 20, comprising the additional

2   steps of [coupling to a global video bus said video data with] connecting the

3   hardware components of the processing module to a crosspoint switch and

4   providing associated video timing [information] signals with the video data, said

5   video timing signals being synchronized to a system clock signal, and routing said

6   video data and [its] associated video timing [information] signals to/from respective

7   parallel pipelined video hardware components of said video processing module over

8   said global video bus via [a] the crosspoint switch, said timing signals indicating

9   when the video data represents active video information [data compensating for

10   pipeline delay in said video processing module].

1   22.   (Amended) The method of claim 21, comprising the additional

2   step of [said processing module] providing at least one synchronous start signal [to

3   each detected video processing module over] via said global control bus said

4   synchronous start signal being coupled to the processing module and to the at least

5   one video processing module to signal the start of the at least one video processing

6   operation.

1   23.   (Amended) The method of claim 22, comprising the additional

2   step of coupling a semaphore register to the processing module said semaphore

3   register being configured to coordinate [coordinating] multitask processing

4   operations when said processing module comprises at least two general purpose

5   microprocessors.

1   24.   (Amended) The method of claim 21, comprising the additional

2   steps of connecting a crosspoint state machine to said crosspoint switch, said

3   crosspoint state machine monitoring transfers of video data over each data path of

4   said crosspoint switch and [facilitating selection of idle data] allocating paths for

5   [each transfer of data from one] transferring the video data among the parallel

6   pipelined video hardware [component to another] components.

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25.   (Amended)   The method of claim 21, wherein said control data
comprises [video device information] <u>respective control signals</u> for each hardware
component of said video processing system, [comprising the further step of said]
<u>the method including the step of coupling said</u> processing module [manipulating] <u>to</u>
<u>manipulate</u> said [video device information] <u>control signals</u> to program said
hardware components for each of said different video processing operations.

26.   (Amended)   The method of claim [21] <u>22</u>, comprising the steps of
<u>configuring the video processing module to</u> automatically [compensating]
<u>compensate</u> for differences in <u>input video timing between respective [images]</u>
<u>combinations of video data and video timing signals provided by said crosspoint</u>
<u>switch</u> and [providing] <u>to provide</u> dual image pointwise video processing operations
and image accumulations of said respective images.

27.   (Amended)   A modular processing system comprising:

at least one specialized processing module which contains parallel
pipelined hardware [which] <u>that</u> is programmable to provide different specialized
processing operations on an input stream of data;

a general processing module containing a general purpose microprocessor
which controls hardware and software operation of said specialized processing
module <u>and said general processing module,</u> using a hardware control library
loaded on said general purpose microprocessor, said hardware control library
comprising a set of functions for programming said parallel pipelined hardware of
said at least one specialized processing <u>module and said microprocessor of said</u>
<u>general processing module</u> to perform predetermined specialized processing
operations <u>on the input stream of data;</u> and

a global control bus which provides control data to/from said hardware
control library of said general processing module from/to said at least one
specialized processing module separate from said <u>stream of</u> input data to be